REMARKS

The Office Action dated January 5, 2009 was received and carefully reviewed.

By this response, claims 1-4 are amended to clarify the invention, and not for reasons of patentability. Claims 10-13 remain withdrawn for being directed to a non-elected invention. No new claims have been added, and no claims have been canceled. Accordingly, claims 1-13 remain pending in the subject application.

Reconsideration and allowance are hereby requested in view of the above amendments and the following remarks.

Claim Rejections - 35 U.S.C. § 112

Claims 1-9 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. However, the amendments to independent claims 1-4 obviate any perceived indefiniteness noted by the Examiner. Accordingly, Applicants hereby request the withdrawal of the rejection.

Claim Rejections - 35 U.S.C. § 102

Claims 1-9 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Fujii et al. (U.S. Pat. Pub. No. 2005/0074963 A1). Applicants traverse this rejection for at least the reasons set forth below.

Applicants respectfully submit that independent claims 1-4, and the claims dependent therefrom, are patently distinguishable over *Fujii*, since *Fujii* fails to disclose, teach, or suggest all of the features recited in the pending claims. For example, new independent claim 1 recites:

> 1. A light-emitting device comprising:
> a light-emitting element in which a light-emitting material is sandwiched between a pair of electrodes in a pixel; and
> a thin film transistor including, from a substrate side, a lamination of:
> a gate electrode formed by fusing conductive nanoparticles;

a gate insulating layer formed in contact with the gate electrode, the gate insulating layer including at least a layer comprising a silicon nitride or a silicon nitride oxide, and a layer comprising a silicon oxide; and

a semiconductor layer,

wherein the light-emitting element and the thin film transistor are connected in the pixel.

Independent claim 2 (emphasis added) recites:

2. A light-emitting device comprising:

a light-emitting element in which a light-emitting material is sandwiched between a pair of electrodes in a pixel; and

a thin film transistor including, from a substrate side, a lamination of:

a gate electrode formed by fusing conductive nanoparticles;

a gate insulating layer formed in contact with the gate electrode, the gate insulating layer including at least a layer comprising a silicon nitride or a silicon nitride oxide, and a layer comprising a silicon oxide;

a semiconductor layer;

wirings connected to a source and a drain and formed by fusing conductive nanoparticles; and

a silicon nitride layer or silicon nitride oxide layer formed by being in contact with the wirings,

wherein the light-emitting element and the thin film transistor are connected in the pixel.

Independent claim 3 (emphasis added) recites:

3. A light-emitting device comprising:

a light-emitting element in which a light-emitting material is sandwiched between a pair of electrodes in a pixel;

a first thin film transistor including, from a substrate side, a lamination of:

a gate electrode formed by fusing conductive nanoparticles;

a gate insulating layer formed in contact with the gate electrode, the gate insulating layer including at least a layer comprising a silicon nitride or a silicon nitride oxide, and a layer comprising a silicon oxide; and

a semiconductor layer;

a driver circuit including a second thin film transistor formed by having the same layer structure as that of the first thin film transistor; and

a wiring extended from the driver circuit and connecting to the gate electrode of the first thin film transistor,

wherein the light-emitting element and the thin film transistor are connected in the pixel.

Independent claim 4 (emphasis added) recites:

4. A light-emitting device comprising:

a light-emitting element in which a light-emitting material is sandwiched between a pair of electrodes in a pixel;

a first thin film transistor including, from a substrate side, a lamination of:

a gate electrode formed by fusing conductive nanoparticles;

a gate insulating layer formed in contact with the gate electrode, the gate insulating layer including at least a layer comprising a silicon nitride or a silicon nitride oxide, and a layer comprising a silicon oxide;

a semiconductor layer;

wirings connected to a source and a drain and formed by fusing conductive nanoparticles; and

a silicon nitride layer or silicon nitride oxide layer formed to be in contact with the wirings;

a driver circuit including a second thin film transistor formed by having the same layer structure as that of the first thin film transistor; and

a wiring extended from the driver circuit and connecting to the gate electrode of the first thin film transistor,

wherein the light-emitting element and the thin film transistor are connected in the pixel.

Thus, independent claims 1-4 are directed to, *inter alia*, the features of a gate insulating layer formed in contact with the gate electrode, the gate insulating layer including at least a layer comprising a silicon nitride or a silicon nitride oxide, and a layer comprising a silicon oxide.

Applicants contend that *Fujii* neither discloses, teaches, nor suggests at least the feature of a gate insulating layer formed in contact with the gate electrode, the gate insulating layer including at least a layer comprising a silicon nitride or a silicon nitride oxide, and a layer comprising a silicon oxide, as recited in independent claims 1-4.

On page 4 of the Office Action, the Examiner alleges that *Fujii* discloses "a gate insulating layer (106) formed in contact with the gate electrode (106) [*sic*], at least containing a

layer comprising a silicon nitride (par. 52)". However, paragraph [0052] of *Fujii* actually recites:

> **[0052]** A gate insulating film **106** is formed over the gate electrode **104** and the scan line **105**. It is preferable that the gate insulating film be formed with an insulating film containing silicon, such as silicon nitride, silicon oxide, by a film formation method such as plasma CVD or sputtering.

As seen above, *Fujii* appears to merely disclose that the gate insulating film 106 may be formed containing "silicon, such as silicon nitride, silicon oxide" (see *Fujii*, e.g., paragraph [0052]). However, *Fujii* is completely silent with regard to "a gate insulating layer formed in contact with the gate electrode, **the gate insulating layer including at least a layer comprising a silicon nitride or a silicon nitride oxide, and a layer comprising a silicon oxide**", as recited (emphasis added) in present independent claims 1-4.

Accordingly, *Fujii* fails to anticipate each and every feature recited in the independent claims. Thus, Applicants respectfully request the withdrawal of the rejection under 35 U.S.C. § 102(e), and the allowance of these claims.

Further, claims 5-9 are allowable at least by virtue of their dependency from one of the independent claims, but also because they are distinguishable over the prior art. Accordingly, Applicants respectfully request the withdrawal of the rejection, and the allowance of these claims.

In view of the foregoing, it is submitted that the present application is in condition for allowance and a notice to that effect is respectfully requested. If, however, the Examiner deems that any issue remains after considering this response, the Examiner is invited to contact the undersigned attorney/agent to expedite the prosecution and engage in a joint effort to work out a mutually satisfactory solution.

Except for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required,

including any required extension of time fees, or credit any overpayment to Deposit Account No. 19-2380. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

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